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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,580	07/21/2003	Scott B. Herner	MA-040-a	7514

7590 03/03/2005

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EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,580	HERNER ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *072103*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 4, 20-24 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-2, 4-5 of U.S. Patent No. 6,635,556 in view of Wang et al (US 6,511,923)

Claims 1-2, 4-5 of US 6,635,556 meets all the limitations of the instant claimed inventions as per claims 4, 20-24 except the limitation of removing the undoped silicon capping layer. Wang discloses a method for forming a stable dielectric films comprises the step of removing the undoped silicon capping layer 18 by CMP (col 6, lines 40-48).

One skilled in the art at the time the invention was made would have found it obvious to modify claims 1-2, 4-5 of US 6,635,556 by adding the step of removing the undoped silicon capping layer as per Wang to produce instant claimed inventions as per claims 4, 20-24 because Wang discloses that a planarization procedure such as CMP is common after dielectric deposition prior to subsequent processing (col 6, lines 38-40)

Present invention claims	US 6,635,556
4	1
20-24	2, 4-5

Claims 7, 8, 10-12, 15-19 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 11-14 of U.S. Patent No. 6,635,556 in view of Choi (US 5,950,109)

Claims 11-14 of US 6,635,556 meets all the limitations of the instant claimed inventions as per claims 7-8, 10-12, 15-19 except the limitation of introducing a second wafer into the pressure vessel after the formation of the undoped capping layer and forming a second silicon layer over the surface of the second wafer. Choi discloses a method for depositing films on semiconductor wafer comprises the step of introducing a second wafer into the pressure vessel and forming a second silicon layer over the surface of the second wafer (col 5, lines 25-30)

One skilled in the art at the time the invention was made would have found it obvious to modify claims 11-14 of US 6,635,556 by adding the step of introducing a second wafer into the pressure vessel and forming a second silicon layer over the surface of the second wafer as per Choi to produce instant claims 7-8, 10-12, 15-19 because Choi discloses that his invention eliminates the need to use dummy wafers and allows the repeated, efficient and continuous loading of sets of active wafers into a deposition apparatus (col 6, lines 49-54)

Present invention claims	US 6,635,556
7-8, 10-12	11-14

15-19 11-14

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5, 25-28, 30-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al (US 6,511,923)

Wang discloses a method for forming dielectric film comprises the steps of:

forming a first in-situ dielectric layer 16/doped silicon layer over a substrate 10 in a pressure chamber while flowing SiF4/precursor gas (col 5, lines 6-24)

forming an undoped silicon capping layer 18 on and in contact with layer 16/doped silicon layer without removing the substrate from the chamber and without flowing SiF4/discontinuing precursor gas (col 5, lines 40-66; fig. 2)

removing/consuming the undoped capping layer 18 by CMP (col 6, lines 40-48; fig. 3)

Wang also discloses using the invention to manufacture NMOS transistor/memory device (col 14, lines 47-53)

The limitations of claims 2, 5, 26 have been discussed above

Regarding claims 3, 28, Wang discloses forming a doped silicon layer 20/second in-situ doped silicon layer (col 6, lines 13-15; col 6, lines 52-55)

Regarding claims 30-31, Wang discloses that the undoped layer 18 having a thickness of 50-200 angstroms is thinner than layer 16/first doped layer (col 6, lines 10-13)

4. Claim 15 is rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al (US 6,511,923)

Wang discloses a method for forming dielectric film comprises the steps of:

forming a first in-situ dielectric layer 16/doped silicon layer over a substrate 10 in a pressure chamber while flowing SiF4/precursor gas (col 5, lines 6-24)

forming an undoped silicon capping layer 18 on and in contact with layer 16/doped silicon layer in-situ without removing the substrate from the chamber and without flowing SiF4/discontinuing precursor gas (col 5, lines 40-66; fig. 2)

forming a second doped silicon 20 on and in contact with layer 18/undoped caaping layer (col 6, lines 13-15). Wang also discloses using the invention to form the dielectric films to manufacture NMOS transistor/memory device (col 14, lines 47-53)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 6, 16-18, 20-23, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al (US 6,511, 923) in view of Hill (US 6,384,466)

Wang's method has been described above. Unlike the instant claimed inventions as per claims 6, 16, 20, 29, Wang fails to specifically disclose forming a three dimension memory array from the transistor/ memory device

Hill discloses a method for forming multi-layer dielectric comprises the step of specifically disclose forming a memory array from the transistor/ memory device having the dielectric layers (col 3, lines 24-30)

One skilled in the art at the time the invention was made would have found it obvious to employ Wang transistor/memory device to form a three dimension memory array in view of Hill teaching because Hills discloses that an assembly includes a number of structure covered with a multi-layer dielectric can be a portion of a memory array (col 3, lines 24-30)

Regarding claims 17-18, 21-22, Wang discloses that the undoped layer 18 having a thickness of 50-200 angstroms is thinner than layer 16/first doped layer (col 6, lines 10-13)

Regarding claim 23, Wang discloses forming a second doped silicon 20 on and in contact with layer 18/undoped capping layer (col 6, lines 13-15)

7. Claims 7-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al (US 6,511, 923) in view of Choi (US 5,950,109)

Wang discloses a method for forming dielectric film comprises the steps of:

forming a first in-situ dielectric layer 16/doped silicon layer over a substrate 10 in a pressure chamber while flowing SiF4/precursor gas (col 5, lines 6-24)

forming an undoped silicon capping layer 18 on and in contact with exposed layer 16/doped silicon layer in-situ without removing the substrate from the chamber and without flowing SiF4/discontinuing precursor gas (col 5, lines 40-66; fig. 2)

Wang discloses that the undoped capping layer 18 having a thickness of 50-200 angstroms (col 6, lines 10-13), which reads on the thickness of the undoped capping layer is sufficient to reduce autodoping in the second silicon layer to approximately a back ground level since the specification (page 12) discloses that "an undoped silicon capping layer having a thickness of 200 angstroms or greater is sufficient to reduce the effects of autodoping to a substantially background level"

Unlike the instant claimed invention as per claims 7, 11, Wang fails to disclose the step of introducing a second wafer into the pressure vessel after the formation of the undoped capping layer and forming a second silicon layer over the surface of the second wafer.

Choi discloses a method for depositing films on semiconductor wafer comprises the step of introducing a second wafer into the pressure vessel and forming a second undoped silicon layer over the surface of the second wafer (col 5, lines 25-30)

One skilled in the art at the time the invention was made would have found it obvious to modify Wang method by adding the step of introducing a wafer into the pressure vessel and forming a second silicon layer over the surface of the second wafer as per Choi because Choi discloses that his invention eliminates the need to use dummy wafers and allows the repeated, efficient and continuous loading of sets of active wafers into a deposition apparatus (col 6, lines 49-54)

Regarding claims 8-10, Wang discloses that the undoped layer 18 having a thickness of 50-200 angstroms is thinner than layer 16/first doped layer (col 6, lines 10-13)

Regarding claim 13, Wang also discloses using the invention to form the dielectric films to manufacture NMOS transistor/memory device (col 14, lines 47-53)

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al (US 6,511, 923) in view of Choi (US 5,950,109) and further in view of Hill (US 6,384,466)

Wang as modified by Choi has been described above. Unlike the instant claimed invention as per claim 14, Wang and Choi fail to specifically disclose forming a three dimension memory array from the transistor/ memory device

Hill discloses a method for forming multi-layer dielectric comprises the step of specifically disclose forming a memory array from the transistor/ memory device having the dielectric layers (col 3, lines 24-30)

One skilled in the art at the time the invention was made would have found it obvious to employ Wang and Choi transistor/memory device to form a three dimension memory array in view of Hill teaching because Hills discloses that an assembly includes a number of structure covered with a multi-layer dielectric can be a portion of a memory array (col 3, lines 24-30)

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LV
March 1, 2005